

IN THE CLAIMS

Please amend the claims as follows:

- 1 1. (original) A circuit testing apparatus comprising:
2 a controller for controlling signals being transferred between a circuit under
3 test and the circuit testing apparatus; and
4 a driver circuit for generating signals to be applied to the circuit under test,
5 the driver circuit includes a high speed slave chain and a DC control loop chain
6 coupled to the circuit under test, the high speed slave chain receives a differential
7 voltage logic pulse train and converts said logic pulse train into an high speed
8 current steering for producing said drive signal to be applied to the circuit under
9 test, the DC control loop chain provides feedback paths for DC regulation of inputs
10 of said high speed slave chain.
- 1 2. (original) The circuit testing apparatus of claim 1, wherein the driver is a class A
2 driver.
- 1 3. (original) The circuit testing apparatus of claim 1, wherein the driver circuit is
2 coupled to a pin on the circuit under test.
- 1 4. (original) The circuit testing apparatus of claim 1, further comprising a receiver circuit
2 for receiving output signals from the circuit under test.
- 1 5. (original) The circuit testing apparatus of claim 4, wherein the receiver circuit is
2 coupled to a pin on the circuit under test.

1 6. (original) The circuit testing apparatus of claim 4, wherein the receiver circuit and the
2 driver circuit are coupled together to a pin on the circuit under test.

1 7. (original) The circuit testing apparatus of claim 1, wherein the high speed slave chain
2 further includes an input clamp stage for receiving said differential logic pulse train and
3 converting said differential logic pulse train into fixed amplitude complimentary output
4 voltages.

1 8. (original) The circuit testing apparatus of claim 1, wherein the DC control loop chain
2 further includes an input clamp stage for receiving fixed differential logic signals and
3 converting said fixed differential logic pulse train into fixed amplitude complimentary
4 output voltages.

1 9. (original) The circuit testing apparatus of claim 8, wherein the high speed slave chain
2 and DC control loop chain further include a current controlled gain stage for receiving
3 fixed amplitude complimentary output voltages of the input clamp stage and employing a
4 controlled cascode translinear multiplier cell configuration to provide a wide bandwidth
5 with high DC precision and low distortion means of controlling the amplitude.

1 10. (original) The circuit testing apparatus of claim 9, wherein the high speed slave chain
2 and DC control loop further includes an output stage that is a standard cascaded differential
3 linear amplifier.

1 11. (currently amended) The circuit testing apparatus of claim 10, wherein the output stage
2 of the high speed slave chain whose output currents drive an output resistor of the said
3 driver circuit.

1 12. (original) The circuit testing apparatus of claim 10, wherein the output stage of DC
2 control loop chain provides feedback currents to DC control loop chain.

1 13. (currently amended) The circuit testing apparatus of claim 1, wherein the high speed
2 slave chain and DC control loop chain further comprises an output stage that includes a
3 differential-input pair of transistors, ~~which~~ where each transistor receives a differential
4 ~~voltage input~~ current as input signal to drive the their respective output stage circuits.

1 14. (currently amended) The circuit testing apparatus of claim 13, wherein the output stage
2 further includes a second pair of transistors, ~~that~~ where each of said second pair of
3 transistors receives a single-ended voltage input.

1 15. (currently amended) The circuit testing apparatus of claim 14, the output stage further
2 includes a resistance coupled between the second pair of transistors, ~~the differential voltage~~
3 ~~input signal controlling an amount of current through the resistance to control a current~~
4 ~~level in each of the transistors to generate the drive signal applied to the circuit under test.~~

1 16. (currently amended) The circuit testing apparatus of claim 14, the output stage further
2 includes a pair of current sources coupled to the second pair of transistors, each of the
3 current sources driving a respective current through a respective one of the second pair of
4 transistors.

1 17. Canceled

1 18. (currently amended) The circuit testing apparatus of claim 9, wherein the second pair
2 of transistors are bipolar junction transistors.

1 19. (original) A circuit testing apparatus comprising:

2 controlling means for controlling signals being transferred between a circuit
3 under test and the circuit testing apparatus; and

1 driving means for generating signals to be applied to the circuit under test,
2 the driver circuit includes a high speed slave chain and a DC control loop chain
3 coupled to the circuit under test, the high speed chain circuit receives a differential
4 voltage logic pulse train and converts said logic pulse train into an high speed
5 current steering for producing said drive signal to be applied to the circuit under
6 test, the DC control loop chain provides feedback paths for DC regulation of inputs
7 of said high speed slave chain.

1 20. (original) The circuit testing apparatus of claim 19, wherein the driver is a class A
2 driver.

1 21. (original) The circuit testing apparatus of claim 19, wherein the driver circuit is
2 coupled to a pin on the circuit under test.

1 22. (original) The circuit testing apparatus of claim 19, further comprising a receiver
2 circuit for receiving output signals from the circuit under test.

- 1 23. (original) The circuit testing apparatus of claim 22, wherein the receiver circuit is
2 coupled to a pin on the circuit under test.
- 1 24. (original) The circuit testing apparatus of claim 22, wherein the receiver circuit and
2 the driver circuit are coupled together to a pin on the circuit under test.
- 1 25. (original) The circuit testing apparatus of claim 19, wherein the high speed slave chain
2 further includes an input clamp stage for receiving said differential logic pulse train
3 and converting said differential logic pulse train into fixed amplitude
4 complimentary output voltages.
- 1 26. (original) The circuit testing apparatus of claim 19, wherein the DC control loop chain
2 further includes an input clamp stage for receiving fixed differential logic signals
3 and converting said fixed differential logic pulse train into fixed amplitude
4 complimentary output voltages.
- 1 27. (original) The circuit testing apparatus of claim 26, wherein the high speed slave
2 chain and DC control loop chain further include a current controlled gain stage for
3 receiving fixed amplitude complimentary output voltages of the input clamp stage
4 and employing a controlled cascode translinear multiplier cell configuration to
5 provide a wide bandwidth with high DC precision and low distortion means of
6 controlling the amplitude.

- 1 28. (original) The circuit testing apparatus of claim 27, wherein the high speed slave
2 chain and DC control loop further includes an output stage that is a standard
3 cascoded differential linear amplifier.
- 1 29. (currently amended) The circuit testing apparatus of claim 28, wherein the output
2 stage of the high speed slave chain whose output currents drive an output resistor of
3 the said driver circuit.
- 1 30. (original) The circuit testing apparatus of claim 29, wherein the output stage of DC
2 control loop chain provides feedback currents to DC control loop chain
- 1 31. (currently amended) The circuit testing apparatus of claim 19, wherein the high
2 speed slave chain and DC control loop chain further comprises an output stage that
3 includes a differential-input pair of transistors, ~~which~~ where each transistor receives
4 a differential voltage input current as input signal to drive the their respective output
5 stage circuits.
- 1 32. (currently amended) The circuit testing apparatus of claim 31, wherein the output
2 stage further includes a second pair of transistors, that where each of said second
3 pair of transistors receives a single-ended voltage input.
- 1 33. (currently amended) The circuit testing apparatus of claim 32, the output stage
2 further includes a resistance coupled between the second pair of transistors, the
3 ~~differential voltage input signal controlling an amount of current through the~~

4 ~~resistance to control a current level in each of the transistors to generate the drive~~
5 ~~signal applied to the circuit under test.~~

1 34. (currently amended) The circuit testing apparatus of claim 33, the output stage
2 further includes a pair of current sources coupled to the second pair of transistors,
3 each of the current sources driving a respective current through a respective one of
4 the second pair of transistors.

1 35. Canceled

1 36. (currently amended) The circuit testing apparatus of claim 31, wherein the second
2 pair of transistors are bipolar junction transistors.

1 37. (currently amended) A method of testing a circuit, comprising:
2 providing a controller for controlling signals being transferred to and from
3 the circuit under test;
4 providing a driver circuit coupled to the circuit under test;
5 receiving a differential voltage logic pulse train; [[and]]
6 converting said logic pulse train into a high speed current steering for
7 producing said a drive signal ~~to be applied to the circuit under test;~~ and
8 performing testing of said circuit under test using said drive sign.

1 38. (original) The circuit testing apparatus of claim 37, wherein the driver circuit is a
2 class A driver.

- 1 39. (original) The circuit testing apparatus of claim 37, wherein the driver circuit is
2 coupled to a pin on the circuit under test.
- 1 40. (original) The circuit testing apparatus of claim 37, further providing a receiver circuit
2 for receiving output signals from the circuit under test.
- 1 41. (original) The circuit testing apparatus of claim 40, wherein the receiver circuit is
2 coupled to a pin on the circuit under test.
- 1 42. (original) The circuit testing apparatus of claim 41, wherein the receiver circuit and
2 the driver circuit are coupled together to a pin on the circuit under test.
- 1 43. (original) The circuit testing apparatus of claim 38, wherein receiving said differential
2 logic pulse train further includes converting said differential logic pulse train into
3 fixed amplitude complimentary output voltages.
- 1 44. (original) The circuit testing apparatus of claim 38, further comprising receiving fixed
2 differential logic signals and converting said fixed differential logic pulse train into
3 fixed amplitude complimentary output voltages.
- 1 45. (original) The circuit testing apparatus of claim 44, further comprising receiving fixed
2 amplitude complimentary output voltages and employing a controlled
3 cascode translinear multiplier cell configuration to provide a wide bandwidth with
4 high DC precision and low distortion means of controlling the amplitude.
- 1 46. (original) The circuit testing apparatus of claim 44, wherein the driver circuit further
2 includes a standard cascoded differential linear amplifier.